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LLC Converters with Planar Transformers: Issues and Mitigation

Mohammad Ali Saket, *Student Member, IEEE,* Navid Shafiei, *Student Member, IEEE,* Martin Ordonez, *Member, IEEE*

***Abstract*—The use of LLC resonant converters has gained popularity in multiple applications that require high conversion efficiency and galvanic isolation. In particular, many applications like portable devices, Flat TVs, and electric vehicle battery chargers require demanding slim-profile packaging and enforce the use of Planar Transformers (PTs) with low-height, low leakage inductance, excellent thermal characteristics, and manufacturing simplicity. The main challenge in successfully designing LLC converters with PT resides in controlling high parasitic capacitances produced by large overlapping layers in PT windings. When the parasitic capacitances are not controlled, they severely impair the converters' performance and regulation, and limit the application of PTs in high frequency LLC converters. This paper characterizes the PT capacitance issue in detail and proposes mitigation strategies to improve the performance of LLC converters with PTs. A systematic analysis is performed, and six PT winding layouts are introduced and benchmarked with a traditional design. As a result of the investigation, an optimized structure is obtained, which minimizes both inter-winding capacitance and AC resistance, while improving the regulation performance of LLC converters. Experimental measurements are presented and show a significant reduction of parasitic capacitance by up to 21.2 intra- and 16.6 inter-winding capacitances, without compromising resistance. This substantial capacitance reduction has a tangible effect on the regulation performance of LLC resonant converters. Experimental results of the proposed PT structure in a 1.2 kW LLC resonant converter show a reduction in common-mode (CM) noise, extended output voltage regulation, and improved overall efficiency of the converter.**

***Index Terms* - LLC resonant converter, voltage regulation, planar transformer, parasitic capacitance, common-mode noise,Finite element analysis (FEA).**

I. Introduction

Growing interests for higher power density and low profile in many low and medium power applications has forced designers to increase switching frequencies. Increasing the frequency reduces the size of passive elements like transformers and inductors, leading to compact power converters. The main obstacle in high frequency operation is switching losses that limits the operating frequency of classical DC-DC PWM hard-switching converters. In order to resolve this issue, soft switching techniques have emerged that minimize the switching loss and allow working in higher frequencies [1–4]. Among different soft-switched converters, the LLC resonant converter offers many advantages including high part-load efficiency, no-load voltage regulation, high gain range over narrow frequency variation, inherent short circuit capability, and good cross regulation [5]. Currently, there are many applications that require high power density and low profile power converters. These applications include and are not limited to consumer electronics (portable devices like laptops and cellphones, Flat TVs), automotive industry (electric vehicle battery chargers and powering), telecom (servers), space and military applications (where rugged and compact power supplies are required). In a high-frequency LLC converter, magnetic components often are the bulkiest parts, and they determine the overall height of the converter [6]. Due to the height of traditional magnetic cores, the form factor of LLC chargers is often plump and bulky. In order to implement slim profile converters for the abovementioned applications, planar transformers (PTs) can be used featuring low height, reproducibility, lower leakage inductance and low thermal resistance [7, 8].

Despite the promising low profile and manufacturing advantages of PTs, their inherent high parasitic capacitances result in severe problems for LLC converters. Fig. 1 (a) presents an LLC resonant converter schematic and includes the parasitic elements of the transformer (leakage inductances, winding resistances, and parasitic capacitances). In particular, parasitic capacitances in the transformers can be divided into inter-winding and intra-winding capacitors, which have a significant detrimental effect in LLC converters as demonstrated in this work. The effect of distributed inter-winding capacitance can be modeled by four capacitors between primary and secondary ports of the transformer which are shown in red color in Fig. 1 (a). The high inter-winding capacitance between primary and secondary provides an undesired low impedance path for CM noise, contributing to EMI issues. Complying with EMI standards requires significant effort to reduce common mode EMI noise, especially if the noise level is high. Usually, high EMI noise requires bulkier filter that consequently increase the volume and cost of the system. In isolated power supplies, reducing inter-winding capacitance decreases CM noise amplitude significantly, simplifies the filter design and shrink the total filter size. On the other hand, the distributed intra-winding capacitance can be modeled as a lumped capacitor between terminals of the coils. These capacitors are showed with the purple color in the Fig. 1 (a). The high intra-winding capacitance gives rise to a high charging current at the transformer input, resulting in lower efficiency and

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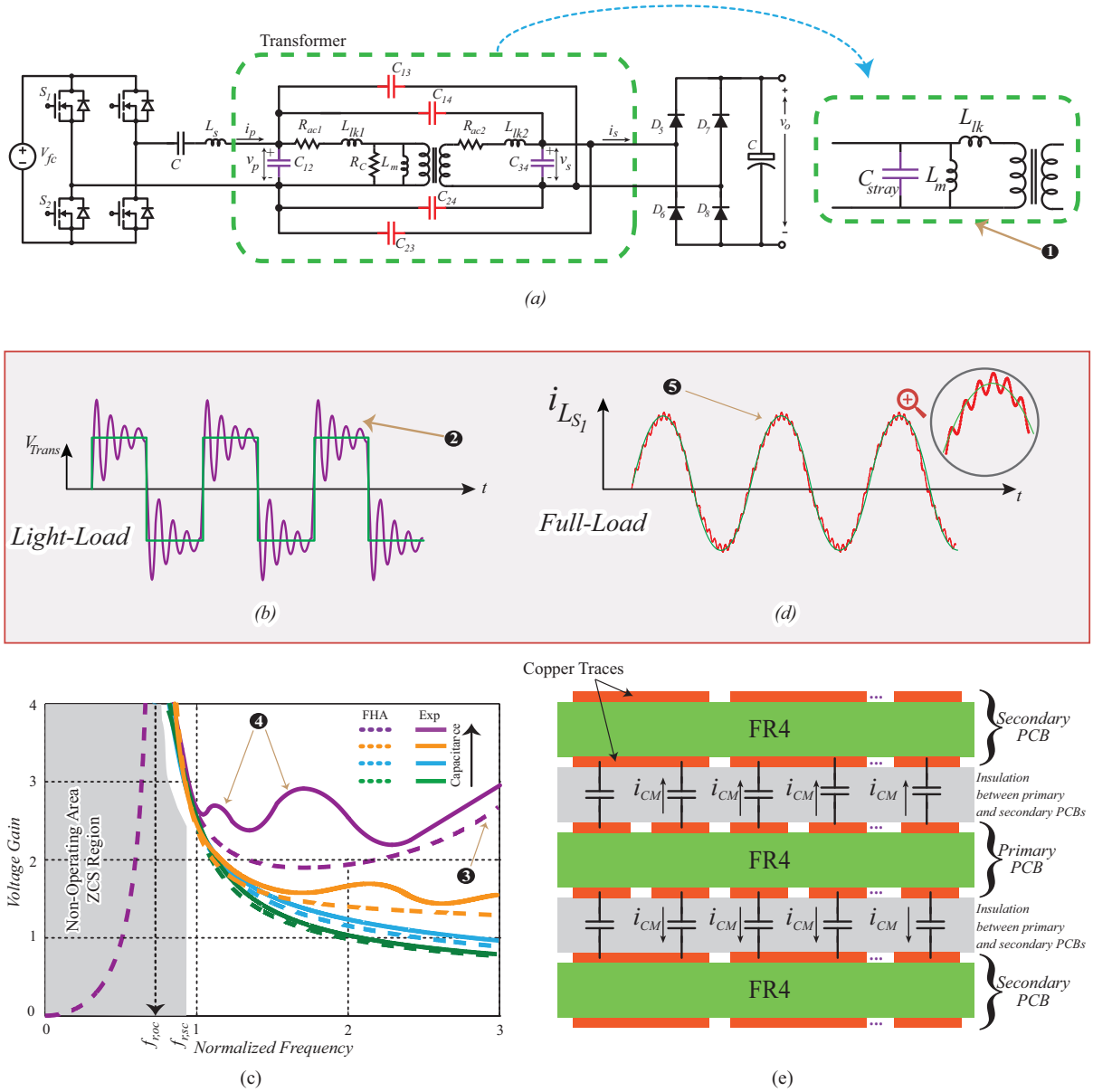


Fig. 1: (a) The LLC resonant converter considering parasitic elements of the transformer and one capacitor model of the transformer ① (b) Transformer distorted no-load voltage due to the stray capacitance ②, (c) The no-load voltage gain characteristics of the converter with different transformers: Unfortunate increase of voltage ③ and deviation of experimental characteristics from FHA prediction with high stray capacitance ④ (d) CM noise problem due to the inter-winding capacitance ⑤, (e) A portion of the transformer consisting of one primary PCB and two secondary PCBs (each PCB is a double layer PCB). The insulation between layers can be FR4, Kapton, or any other material that can provide insulation. This figure shows CM noise currents that result from distributed parasitic capacitances between primary and secondary traces.

increased peak voltage stress across secondary rectifying devices [14]. In addition to those problems, parasitic capacitances also bring unwanted regulation issues for LLC resonant converters with wide output regulation. Voltage regulation is a critical specification in power converters to accommodate input voltage fluctuations (e.g., line regulation) or output voltage changes (e.g., battery chargers). High parasitic capacitance of transformer severely distorts the light-load current and voltage waveforms of the converter, leading to an unpredictable behaviour of output voltage which cannot be seen by First harmonic approxiamation (FHA). A typical waveform of transformer voltage in this condition is presented in Fig. 1 (b). Since the requirement of applying FHA in resonant converters is having square shape voltage and sinusoidal current of the same frequency, applying FHA under this condition leads to inaccurate

results. Solid and dashed curves in Fig. 1 (c) present the light-loading voltage gain characteristics of the LLC resonant converter with experimental measurements and FHA for different values of stray capacitance, respectively. The solid curves clearly show that large parasitic capacitances leads to an unpredictable behavior of output voltage and therefore, loss of the regulation. This figure also shows that although FHA can predict an unfortunate increase in the voltage gain due to the parasitic capacitances which limit the ability of the converter to handles low conversion ratios (e.g., low output voltages or high input voltage), it fails to accurately predict the output voltage. As it is mentioned before, this discrepancy in the results are due to parasitic capacitances that distort the voltage and current waveforms and lead to regulation problems for LLC resonant converters. It is worthy to mention that the FHA curves are found by combining the effect of all parasitic capacitance into one parallel stray capacitance that is showed in Fig. 1 (a). The required equations for getting the value of this stray capacitance based on the six capacitors model of the transformer will be presented in the next sections. Reducing the value of this capacitor can significantly improve the situation and resolve the regulation problem.

During last few years, interesting research has been done to design high efficiency PT for LLC [8–20]. Most of these papers have focused on the AC resistance and leakage inductance, so the impact of transformer parasitic capacitance on the LLC voltage regulation is not covered which is the aim of this paper. Generally speaking, there is a trade-off between PT resistance and parasitic capacitance. In order to have a high efficiency LLC converter with wide output regulation, both parasitic capacitance and AC resistance should be minimized. It is interesting to note that the root cause of LLC regulation problems using PTs has not been addressed in detail in the past. The strategies proposed in this paper provides a solution for light-loading regulation while ensuring high efficiency under full load condition. Since the voltage regulation problem of LLC resonant converter also can be aroused from the rectifier diode junction capacitance, [21–23] have developed methods to address this problem. The work in [21] developed a higher order topology that can mitigate the effect of diode junction capacitances for different modes of operation. Research in [22] suggests that adding a dummy load can solve the problem for small values of diode junction capacitance. The work in [23] presents another mitigation strategy by adding a capacitor to the primary side. Although the prior methods are successful in resolving the regulation issue due to the diode junction capacitance, their effectivity is limited to the values in the range of diode junction capacitance. Since the parasitic capacitance of PTs are much larger, preceding methods cannot be used to resolve the regulation problem due to PTs parasitic capacitance. For instance, the work in [8] reports stray capacitances in the order of few nanoFarads for conventional PTs which results in serious regulation problems in the LLC resonant converters. The work in [24] develops an interesting comb-shaped Faraday shield that reduces the CM noise by roughly halving the inter-winding capacitance. However, in order to mitigate the LLC voltage regulation problem, the parasitic capacitance should be reduced more. The work in [25] developed a minimized overlapping winding layout to reduce the inter-winding capacitance. But the impact on the voltage regulation is not the focus of that work. In addition, no investigation of DC and AC resistance of the layout was provided. Indeed, no overlapping strategy leads to very high AC resistance which limits its usability in high-efficiency applications. Although many papers have discussed different aspects of using PTs in LLC resonant converter, a paper that resolve the light-loading voltage regulation problem along high full load efficiency still is missing in the literature.

This paper characterizes PT capacitance issue in detail and proposes mitigation strategies to improve the performance of LLC converters with PTs. A systematic analysis is performed, and six PT winding layouts are introduced and benchmarked with a traditional design. As a result of the investigation, an optimized transformer is obtained to minimize PT parasitic capacitance while maintaining low AC resistance. For each proposed winding layout, the analytical equations describing the parasitic capacitance are found, and the advantages and disadvantages of each layout are presented. In addition to the proposed winding layouts and arrangement, a comprehensive procedure to extract all parasitic elements of PTs are provided, which can be used to run Finite elements analysis (FEA) simulations of the electro- and magneto-static behavior of PTs. Experimental results show that the proposed transformers have up to 21.2 and 16.6 times less intra- and inter-winding capacitance, without compromising the resistance. This significant parasitic capacitance reduction considerably improves the performance of the converter. Experimental results of employing the proposed transformers in a 1.2 kW LLC resonant converter show that the proposed transformers can successfully resolve both CM noise and voltage regulation problem in the LLC resonant converter and can regulate the output voltage even in the no-load condition. In addition to these benefits, the converter efficiency increases due to elimination of the parasitic capacitance.

This paper is organized into six Sections. In Section II, the equivalent circuit of the transformer is studied, and a comprehensive methodology to extract all parasitic elements with FEA is proposed. Section III proposes six improved winding layouts to strongly reduce the parasitic capacitance. Section IV is dedicated to finding an optimized structure of transformer concerning AC resistance and inter-winding capacitance. Section V provides experimental results and finally, the conclusion is presented in Section VI.

II. Transformer parasitic calculation

As describe in the introduction, high parasitic capacitances of the transformer have severe detrimental effect on the voltage regulation and CM noise of the LLC resonant converter. In order to attain high conversion efficiency and wider output regulation in LLC resonant converters, PT stray capacitances should be minimized as much as possible while keeping AC resistance low. To achieve these goals, a complete method is presented in this section to model of the electro- and magneto-static behavior of the transformer. A comprehensive study of transformer parasitic elements are presented and a full procedure of getting the equivalent circuit using numerical methods are proposed with the objective of designing low parasitic PT to address regulation problems in LCC converters.

A. Parasitic Capacitance

While the transformer is a two-port system from the magnetostatic perspective, the inter-winding capacitance between primary and secondary winding provides a path between primary and secondary, making the transformer a three-port system from the electrostatic standpoint [28]. For a three-port system, three independent voltages and six capacitors are needed to model the electrostatic behaviour of the system. Fig. 2 (a) shows one way of selecting the independent voltages and the six capacitors model of the transformer.

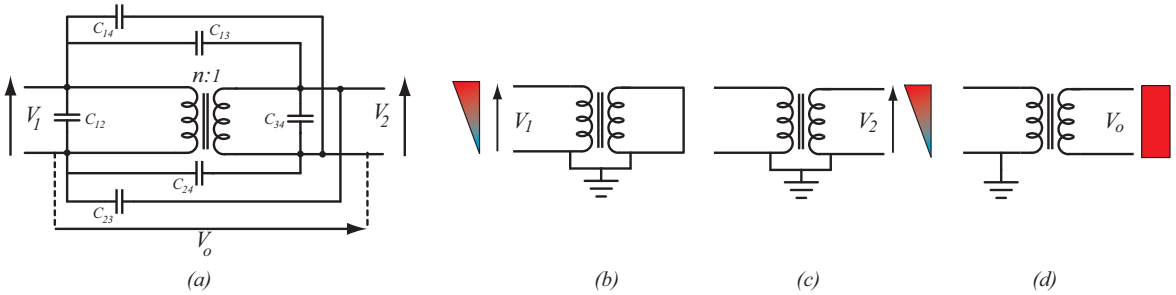


Fig. 2: Electrostatic behavior model of the transformer: (a) Six capacitors model with three independent voltages, (b), (c), and (d) the required numerical analysis to find the six capacitors.

The total energy of the system can be found by summing the energies of the lumped capacitors. In this condition, the total energy of the system is equal to (1).

$$W_t = \frac{1}{2}C_{12}V_1^2 + \frac{1}{2}C_{34}V_2^2 + \frac{1}{2}C_{24}V_o^2 + \frac{1}{2}C_{14}(V_1 - V_o)^2 + \frac{1}{2}C_{23}(V_2 + V_o)^2 + \frac{1}{2}C_{13}(V_1 - V_o - V_2)^2 \quad (1)$$

By rearranging (1) based on voltages, (2) can be obtained.

$$W_t = \frac{1}{2}(C_{12} + C_{14} + C_{13})V_1^2 + \frac{1}{2}(C_{34} + C_{23} + C_{13})V_2^2 + \frac{1}{2}(C_{24} + C_{14} + C_{23} + C_{13})V_o^2 + (-C_{14} - C_{13})V_1V_o + (C_{23} + C_{13})V_2V_o + (-C_{13})V_1V_2 \quad (2)$$

The total energy of the system also can be computed using electric fields. Since MAXWELL equations are linear, they satisfy the superposition principle. In a system with three independent voltages, like the one in Fig. 2 (a), the total electric field is equal to the sum of $\overrightarrow{E_1}$, $\overrightarrow{E_2}$, and $\overrightarrow{E_o}$, corresponding with the voltages $\overrightarrow{V_1}$, $\overrightarrow{V_2}$, and $\overrightarrow{V_o}$. Therefore, the total electric field and electric displacement field in the system can be written as follows:

$$\overrightarrow{E_t} = \overrightarrow{E_1} + \overrightarrow{E_2} + \overrightarrow{E_o} \qquad \overrightarrow{D_t} = \overrightarrow{D_1} + \overrightarrow{D_2} + \overrightarrow{D_o} \quad (3)$$

The total electrostatic potential energy may be expressed in terms of these fields in the form of following equation:

$$\begin{aligned} W_t &= \frac{1}{2}\oint_V (\overrightarrow{E_1} + \overrightarrow{E_2} + \overrightarrow{E_o}).(\overrightarrow{D_1} + \overrightarrow{D_2} + \overrightarrow{D_o})\,dV \\ &= \frac{1}{2}\oint_V \overrightarrow{E_1}.\overrightarrow{D_1} + \frac{1}{2}\oint_V \overrightarrow{E_2}.\overrightarrow{D_2}\,dV + \frac{1}{2}\oint_V \overrightarrow{E_o}.\overrightarrow{D_o}\,dV \\ &+ \frac{1}{2}\oint_V (\overrightarrow{E_1}.\overrightarrow{D_2} + \overrightarrow{E_2}.\overrightarrow{D_1})\,dV + \frac{1}{2}\oint_V (\overrightarrow{E_1}.\overrightarrow{D_o} + \overrightarrow{E_o}.\overrightarrow{D_1})\,dV \\ &+ \frac{1}{2}\oint_V (\overrightarrow{E_2}.\overrightarrow{D_o} + \overrightarrow{E_o}.\overrightarrow{D_2})\,dV \end{aligned} \quad (4)$$

Numerical methods like FEA can be employed to calculate the energy with (4). Three different analyses are required to find all six components which are presented in the Fig. 2 (b), (c) and, (d). The cases presented in the Fig. 2 (b) and (c) require a linear voltage distribution on the turns of one winding, and zero voltage on all the turns of the other winding. The linear distribution of the voltage on turns of one side is signified by a triangle beside that winding. The analysis performed in Fig. 2 (d) requires a constant voltage on all turns of the secondary side and zero voltage on all turns of the primary side. Constant Voltage on all turns of the secondary side also is signified by a square beside that winding, which shows that there is no voltage difference between the terminals of the secondary side. Obtaining the value of the first three terms in (4) are straightforward. The total electrostatic energy in the fig. 2 (b), (c) and (d) are equal to the first, second, and, third terms, respectively. The remaining three components are found using superposition theorem.

Similar to (2), equation (4) indicates that the total energy is composed of six components. Equating corresponding terms in (4) and (2), the expressions for finding the six capacitors are presented in table I. Among the six capacitances, C_{13}, C_{14}, C_{23}, and C_{24} are the inter-winding capacitances and C_{12} and C_{24} model the intra-winding capacitance of the windings. As it is mentioned before, reducing the inter-winding capacitances can significantly attenuate CM noise and enhance the performance of the converter.

TABLE I: Equations describing parasitic capacitances based on the field analysis

Capacitor	*Equation*
C_{13}	$\frac{-1}{2V_1V_2}\oint_V(\overrightarrow{E_1}.\overrightarrow{D_2} + \overrightarrow{E_2}.\overrightarrow{D_1})\,dV$
C_{14}	$\frac{-1}{2V_1V_o}\oint_V(\overrightarrow{E_1}.\overrightarrow{D_o} + \overrightarrow{E_o}.\overrightarrow{D_1})\,dV - C_{13}$
C_{23}	$\frac{1}{2V_2V_o}\oint_V(\overrightarrow{E_2}.\overrightarrow{D_o} + \overrightarrow{E_o}.\overrightarrow{D_2})\,dV - C_{13}$
C_{12}	$\frac{1}{V_1^2}\oint_V(\overrightarrow{E_1}.\overrightarrow{D_1})\,dV - C_{14} - C_{13}$
C_{34}	$\frac{1}{V_2^2}\oint_V(\overrightarrow{E_2}.\overrightarrow{D_2})\,dV - C_{13} - C_{23}$
C_{24}	$\frac{1}{V_o^2}\oint_V(\overrightarrow{E_o}.\overrightarrow{D_o})\,dV - C_{13} - C_{23} - C_{14}$

In order to evaluate the overal impact of parasitic capacitances on the voltage regulation, the six capacitors should be converted to the one capacitor model of Fig. 3 (b). The expressions for calculating this capacitance depends on the connection of primary and secondary windings and different offset voltages lead to different expressions for this capacitance. For the case that there is no external connection between the primary and secondary windings, the offset voltage can be found and the six capacitors model can be reduced to the three capacitor model of Fig. 3 (a) [28]. if the leakage inductances are negligible in comparison to the

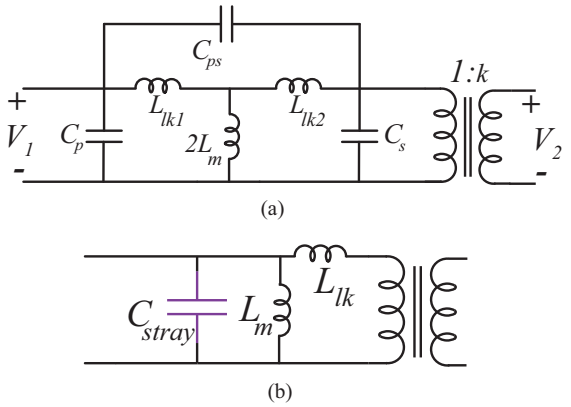


Fig. 3: (a) Three Capacitors model of the transformer referred to the primary side and (b) single capacitance model of the transformer.

magnetizing inductance, the three capacitor model of Fig. 3 (a) can be simplified further to the one capacitor model of Fig. 3 (b) [26]. Under this condition, the expression for the stray capacitance in this circuit has been presented in 5.

$$C_{stray} = C_{12} + k^2 C_{34} + 2k\left(\frac{(C_{14}C_{23} - C_{13}C_{24})}{C_{13}+C_{14}+C_{23}+C_{24}}\right) + \left(\frac{(C_{14}+C_{13})(C_{23}+C_{24}) + k^2(C_{13}+C_{23})(C_{14}+C_{24})}{C_{13}+C_{14}+C_{23}+C_{24}}\right) \quad (5)$$

Where k is the transformer turns ratio. (5) shows that both intra- and inter-winding capacitances contribute to the parallel stray capacitance which leads to regulation problems. Therefore, both types of capacitances should be minimized to reduce the value of this capacitance and solve the voltage regulation problem in the LLC resonant converter.

Equation (5) and table I are useful tools in designing low parasitic capacitance PTs for LLC resonant converter. These equations can be used along FEA to investigate the parasitic capacitance of any design. Regarding CM noise, these equations split the inter-winding capacitance to the four capacitors of C_{13}, C_{14}, C_{23} and, C_{24} which is a great advantage in CM noise modeling. Regarding the voltage regulation problem, (5) can be used to evaluate the value of parallel stray capacitance and avoid the problem of voltage regulation in the LLC resonant converters.

B. AC Resistance and Leakage Inductance Modeling

In order to design an optimized PT for LLC resonant converter, not only the parasitic capacitances should be minimized, but also the AC resistance and leakage inductance of the transformer should be kept low. Therefore, it is also important to define a procedure for finding the AC resistance and leakage inductance of the transformer. In addition to the analytical equations, a procedure of extracting the value of these parasitic elements using numerical tools also is presented.

AC resistance in high frequencies depends on the skin and proximity effects. These two effects are summarized in the Dowels formula to calculate the AC resistance that is presented in the (6).

$$R_{ac} = R_{dc} \times \frac{\xi}{2}\left[\frac{sinh(\xi)+sin(\xi)}{cosh(\xi)-cos(\xi)} + (2m-1)^2 \times \left(\frac{sinh(\xi)-sin(\xi)}{cosh(\xi)+cos(\xi)}\right)\right] \quad (6)$$
$$\xi = \frac{h}{\delta} \qquad m = \frac{F(h)}{F(h)-F(0)}$$

Where h is the thickness of traces, δ is the skin depth at the operating frequency, and F(h) and F(0) are the magneto-motive force (MMF) at the borders of conductor which depend on the structure of the transformer. The first term in (6) is associated with the skin effect and only depends on the ratio of tracks thickness to skin depth ξ. The second term in (6) represents the proximity effect and depends on two factors; ξ and m. The value of m depends on the MMF distribution and is a function of transformers arrangement. It is very crucial to limit the value of m because the proximity effect can increase exponentially and dominate AC resistance. Low m values are achieved in the interleaved structures, where large leakage fluxes are avoided. When the windings are in series, the currents in the windings are the same, yielding in the same magnetic fields along each layer. Under this condition, the MMF distribution changes linearly and is predictable. Due to the predictability of MMF distribution, equation (6) could be used to predict AC resistance. However, When the windings are in parallel, the currents in each winding layer may not be equally distributed due to the leakage fluxes and the high-frequency eddy current effect. On the other hand, AC resistance of each winding is a function of current distribution. This mutual dependency makes it complex to analytically find MMF distribution for parallel layers. Besides, With the parallel connection of windings, it is also possible that circulating currents exist in the parallel layers, causing additional winding loss. As a result, numerical methods like FEA should be used in this condition to find the most optimum structure with the lowest resistance.

Neglecting the capacitive effects, the transformer is a two port system whose equivalent circuit is shown in the Fig. 4 (a). For a two-port system, the relationship between primary and secondary voltages and currents can be represented by a 2×2 matrix. However, finding the matrix impedance of Fig. 4 (a) is not straightforward. Thus, a minor circuit transform is required to get the impedance matrix. The parallel core resistance and magnetizing inductance can be converted to the series from using (7). Fig 4 (b) shows the modified equivalent circuit.

$$L_{ms} = \frac{Q^2}{Q^2+1} \times L_m \;\; , \;\; R_{cs} = \frac{1}{Q^2+1} \times R_c \;\; , \;\; Q = \frac{\omega L_m}{R_c} \quad (7)$$

The matrix representation of this circuit is expressed in 8 and 9.

$$Z = \begin{bmatrix} R_{11}+sL_{11} & R_{12}+sL_{12} \\ R_{21}+sL_{21} & R_{22}+sL_{22} \end{bmatrix} \quad (8)$$

Where

$$\begin{aligned} R_{11}+sL_{11} &= (R_{ac1}+R_{cs}) + S(L_{lk1}+L_{ms}) \\ R_{12}+sL_{12} &= R_{21}+sL_{21} = \frac{1}{n}(R_{cs}+SL_{ms}) \\ R_{22}+sL_{22} &= (R_{ac2}+\frac{1}{n^2}R_{cs}) + S(L_{lk2}+\frac{1}{n^2}L_{ms}) \end{aligned} \quad (9)$$

Arrays of matrix impedance can be found using field analysis which can be done by aid of FEA. (10) and (11) present the elements of

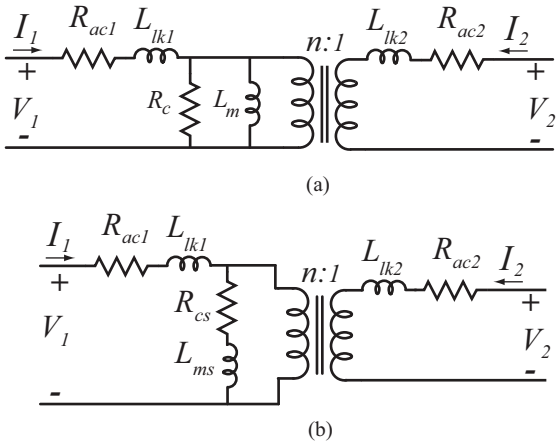


Fig. 4: (a) Transformer equivalent circuit neglecting the capacitive effects and (b) Modified equivalent circuit.

each array based on the fields.

$$R_{ij} = \frac{1}{2 \times I_{i(pk)} \times I_{j(pk)}} \oint_V (\vec{J_i}.\vec{J_j^*} + \vec{J_i^*}.\vec{J_i})\, dV \tag{10}$$

$$L_{ij} = \frac{1}{2 \times I_{i(pk)} \times I_{j(pk)}} \oint_V (\vec{H_i}.\vec{H_j^*} + \vec{H_i^*}.\vec{H_i})\, dV \tag{11}$$

In the above equations, J_i and H_i are the current density and magnetic field due to the input current at the port i. Besides, the R_{ij} and L_{ij} are resistance and inductance associated with the array ij in the impedance matrix. In the case of two windings transformer, there are two ports and two different analysis are required to get corresponding current densities and magnetic fields. In finding field solution, eddy currents should be considered to investigate the impact of arrangement on the AC resistance and leakage inductance. After finding field solution for each case, superposition theorem will be used to calculate the (10) and (11). Equating the matrix produced with these equations with the transformer impedance matrix, the values of equivalent circuit can be found by (12).

$$\begin{aligned} R_{ac1} &= R_{11} - \frac{1}{k}R_{12} & L_{lk1} &= L_{11} - \frac{1}{k}L_{12} \\ R_{ac2} &= R_{22} - kR_{21} & L_{lk2} &= L_{22} - kL_{21} \\ L_{ms} &= \frac{1}{k}L_{12} & R_{cs} &= \frac{1}{k}R_{12} \end{aligned} \tag{12}$$

Having the required analysis to extract the PT parasitic elements, it is possible to design optimized PTs with low parasitic elements for the LLC resonant converter. These analysis tools are used through this paper to investigate different PT structures and designing low parasitic capacitance PTs for the LLC resonant converter with wide output voltage regulation.

III. Reduction of the Parasitic Capacitances

As discussed in this paper, the performance of LLC resonant converters considerably degrades in the presence of the transformer parasitic capacitances. The inter-winding capacitance make the CM noise problem and the primary stray capacitance leads to voltage regulation problem under light-loading condition. Therefore, efforts should be made to minimize the stray capacitance of PT in the design stage. However, reducing the parasitic capacitance often leads to increment in resistance. Therefore, both of these parasitic elements should be considered at the same time to achieve high-efficiency and low-parasitic PT. In this section, a systematic analysis is performed, and six PT winding layouts are introduced and benchmarked with a traditional design. The analysis starts with the static capacitance between two layers of the traditional spiral winding layout and then the low parasitic capacitance layouts are introduced.

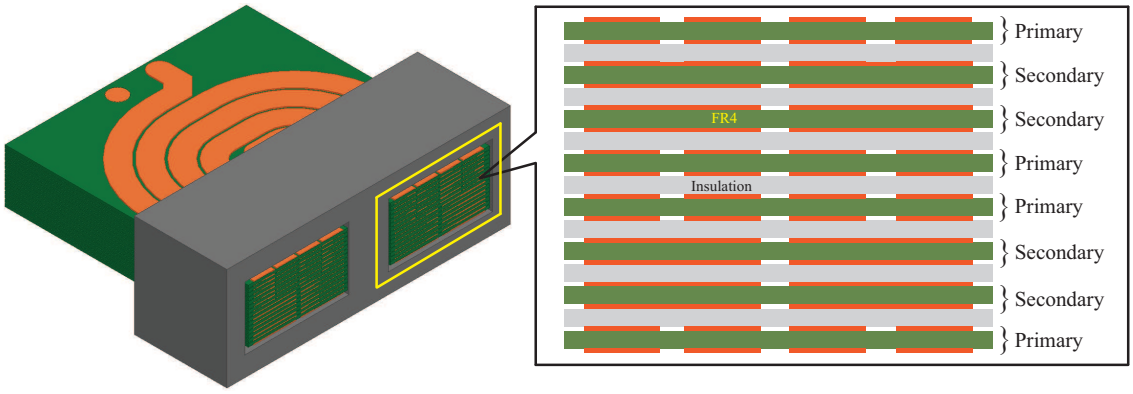
The value of the static capacitance between two conductive layers with overlapping area of A_t and separation distance of d is presented in (13).

$$C_{static} = \epsilon_0 \epsilon_r \frac{A_t}{d} \tag{13}$$

Where ϵ_r is the permittivity of the material between layers. For a transformer with m intersections of primary and secondary, the total value of static inter-winding capacitance is presented in (14).

$$C_{static} = m \times \epsilon_0 \epsilon_r \frac{A_t}{d} \tag{14}$$

The total value of the inter-winding capacitance is equal to the sum of C_{13}, C_{14}, C_{23} and, C_{24} capacitors. Therefore, reducing the total value of inter-winding capacitance means that the overall impact of inter-winding capacitance is reduced. Equation (14) shows that the total value of static inter-winding capacitance can be reduced by increasing the separation distance, reducing the overlapping area, reducing the number of intersections, and using low permittivity materials between layers. Increasing the separation distance reduces the value of capacitance. However, more distance means more space for insulation and less space for copper that leads to higher conduction losses. As a result, this method often sacrifices resistance to reduce the parasitic capacitance. Reducing the overlapping area also reduces the PCB utilization and increase the DC resistance. Also, this method suffers from high proximity effect that results in very high AC resistance. Therefore, among different factors, only number of intersections and the permittivity of the material can be manipulated to reduce the static inter-winding capacitance. Reducing the number of intersections should be done by considering the proximity effect. While the non-interleaved (NI) structure has only one intersection, it cannot be used due to the high ratio of AC to DC resistance. The proposed methods and procedures in the previous section can be used to find an optimized transformer arrangement that minimize both AC resistance and inter-winding capacitance. Using low permittivity material is a very effective method of reducing the static capacitance with no penalty on the other parasitics. It should be mentioned that FR4 is the most widely used material for PCBs due to its electrical and mechanical properties. This material is flame resistant and provides up to 20 kV/mm electrical insulation. Despite these advantages, FR4 has a relatively high permittivity of 4.7. This high permittivity leads to a considerable parasitic capacitance between top and bottom traces. Since commercial PCBs are usually manufactured using FR4, the parasitic capacitance between top and bottom traces cannot be reduced by using another material. However, we are still able to use low permittivity materials between separate PCBs to reduce the parasitic capacitance between them. This option is only available in the windings realized by modularly stacked double layers PCBs, as the material between PCBs are not necessarily $FR4$. As a result, the windings made with the double layers PCBs are more customizable and capable of reducing the parasitic capacitance than windings that are manufactured by multi-layers PCBs. In



(a) (b)

Fig. 5: (a) The 3D model of a traditional $8:4$ planar transformer with spiral winding and (b) 2D cross section of the transformer showing the arrangement of the transformer. Each primary PCB has eight turns (four on each side) and each secondary PCB has four turns (two on each side). The primary PCBs are connected in parallel and secondary PCBs also are connected in parallel.

order to explain how the material between the PCBs affects the distributed parasitic capacitances, a cross section of an $8:4$ transformer is showed in the Fig. 5 (a) and (b). The primary has four PCBs in parallel and each PCB has eight turns (four on the top and four on the bottom). The secondary also has four PCBs in parallel and each PCB has four turns. Fig. 5 (b) shows a 2D cross section of the transformer and explains how the PCBs are arranged. There are four intersections of primary and secondary PCBs. The material that is used in these intersections significantly affects the interwinding capacitance. In the multi layer PCBs, this material is $FR4$. However, in the winding that are made with double layer PCBs, low permitivity materials like air can be used. Figures 6 (a) and (b) show one of these intersections with $FR4$ and air used, respectively. These figures show that replacing $FR4$ with air reduces the static capacitance between successive PCBs roughly 4.7 times for the same structure. The work in [24] reports that inserting shield can reduce the inter-winding capacitance up to two times. Therefore, inserting air at the intersections is roughly 2.5 times more effective than inserting the shield. The air separation can be realized using hollow frames. Fig. 7 shows an example of frame that can be used to provid air separation between layers. Although air effectively reduces the static capacitance between successive layers, it cannot provide the required insulation clearance between overlapping traces. Therefore, the required insulation clearance between layers can be realized by using one or two layers of Kapton tape.

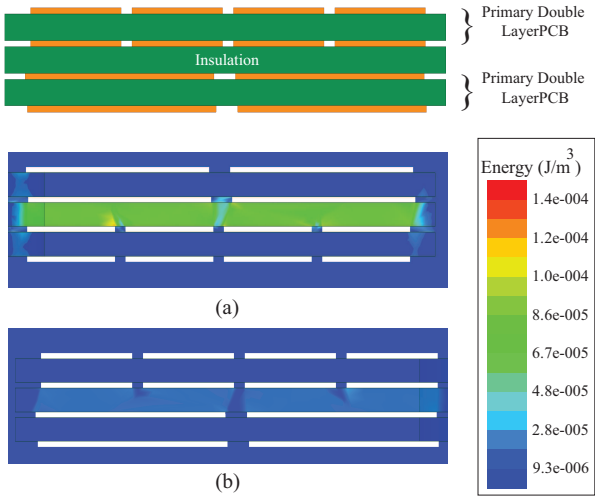


Fig. 6: Inter-winding energy associated with one intersection of primary and secondary. All of the primary turns have voltage equal to 1V and all of the secondary turns have 0V. The energy distribution: (a) with FR4 between PCBs $101pJ$ and (b) with air between PCBs $25pJ$.

Unlike inter-winding capacitance, finding the self-capacitance of two overlapping layers of the same winding requires calculating the total electrostatic energy in that layer. Fig. 8 shows a double sided PCB used as a winding in PTs. The analytical expressions for calculating the intra-winding energy between overlapping traces and adjacent turns are presented in the (15) and (16).

$$E_{overlap} = \int_0^L \frac{1}{2}\epsilon_0\epsilon_r \frac{W \times dx}{d}(\frac{V_w}{L}x)^2 = \frac{1}{6}\epsilon_0\epsilon_r \frac{W \times L}{d}V_w^2 \tag{15}$$

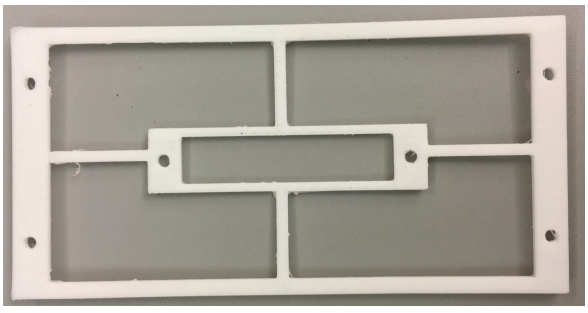
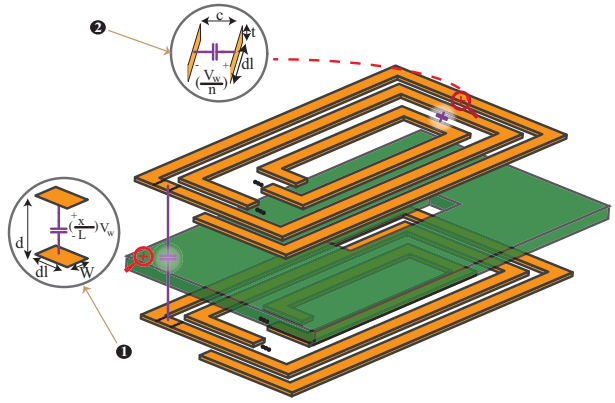


Fig. 7: Example of the frame that is used for air separation.



(a)

(b)

Fig. 8: (a) Traditional spiral winding layout: The distributed capacitance due to overlapping traces ①, the distributed capacitance between adjacent turns at the same side ② and (b) simplified view of the overlapping traces.

$$E_{adjacent} = \int_0^{(1-\frac{2}{n})L} \epsilon_0 \frac{t \times dx}{c} (\frac{V_w}{n})^2 = \epsilon_0 \frac{(n-2)}{n^3} \frac{t \times L}{c} V_w^2 \tag{16}$$

The parameters of (15) and (16) are presented in the table II. The

TABLE II: Parameters definition

Parameter	Definition
L	Total lenght of turns in one side
W	Width of traces
d	Distance between two layers
c	Clearance between adjacent traces
t	Thickness of Copper
n	Total number of turns in PCB
ϵ_r	FR4 permitivity
A_t	Total area of turns

sum of these energies is equal to the energy stored in the lumped intra-winding capacitance. Equating the energy expressions, the value of lumped capacitor can be found using (17).

$$C_{intra} = \frac{1}{3}\epsilon_0\epsilon_r \frac{A_t}{d} + \frac{2(n-2)}{n^3}\epsilon_0 \frac{t}{W}\frac{A_t}{c} \tag{17}$$

In the equation above, the first term is associated with the overlapping turns and the second term shows the intra-winding capacitance due to the adjacent turns of the same side of PCB. In developing the second part, the fringing of electric field is ignored. In reality, due to the fringing of electric field, part of electric field reaches to the adjacent trace through the PCB. Therefore, the value of the second term is higher than what (17) predicts. However, since the thickness of the traces is much smaller than their width and the value of the second term is roughly proportional to $\frac{1}{n^2}$, the value of the second term is negligible in comparison to the first term. For the studied prototypes, the second term is less than three percents of the first part. Ignoring the second part, the intra-winding capacitance of Fig. 8 is presented in the (18).

$$C_{intra} \approx \frac{1}{3}\epsilon_0\epsilon_r \frac{A_t}{d} = \frac{1}{3}C_{static} \tag{18}$$

Equation (18) indicates that for the same area, the value of intra-winding capacitance of two overlapping layers of Fig. 8 is equal to one-third of the static capacitance between two layers. Since replacing $FR4$ with air only is applicable between different PCBs, this method cannot be used to reduce the capacitance between traces of the same PCB. However, in the case that PCBs of the same windings are placed next to each other, air can reduce the value of static capacitance between layers of different PCBs. Figures 9 (a) and (b) show the intra-winding energy of two successive PCBs of the same winding with $FR4$ and air between PCBs, respectively. These figures confirm that air only can mitigate the intra-winding capacitance between layers of different PCBs. In other words, the overall impact of this method on the intra-winding capacitance is much lower. Therefore, other methods should be used to reduce the intra-winding capacitance between traces of the same PCB.

In the following subsections, six improved winding layouts with very low parasitic capacitances are proposed and compared regarding the parasitic capacitance and resistance. These winding layouts are shown in the figures 10 (b), (c), (d), (e), (f), and (g). For each winding layout, the analytical expressions describing DC resistance and intra-winding capacitance are proposed and verified with the aid of FEA. In comparison to the traditional spiral winding layout, the proposed layouts have up to 21.2 and 16.6 less intra- and inter-winding capacitances which significantly reduce the CM noise and solves the regulation problem in the LLC resonant converter, which is the objective of this paper.

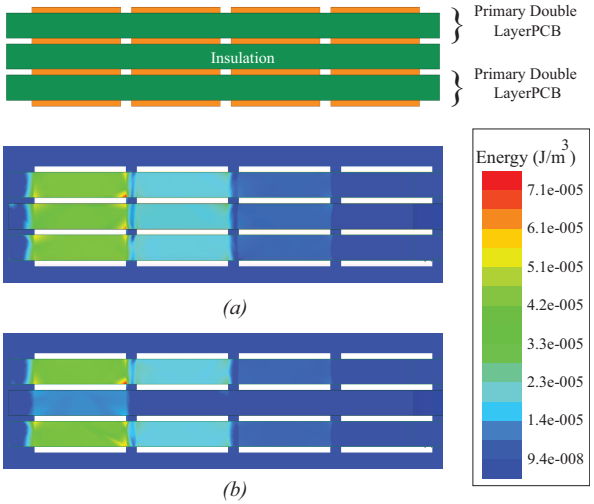


Fig. 9: Intra-winding energy of associated with PCBs of the same winding placed next to each other. The PCBs are connected in parallel and 1V is distributed linearly between terminals of each PCB. Electrostatic energy distribution: (a) with FR4 between PCBs $99pJ$ and (b) with air between PCBs $73pJ$.

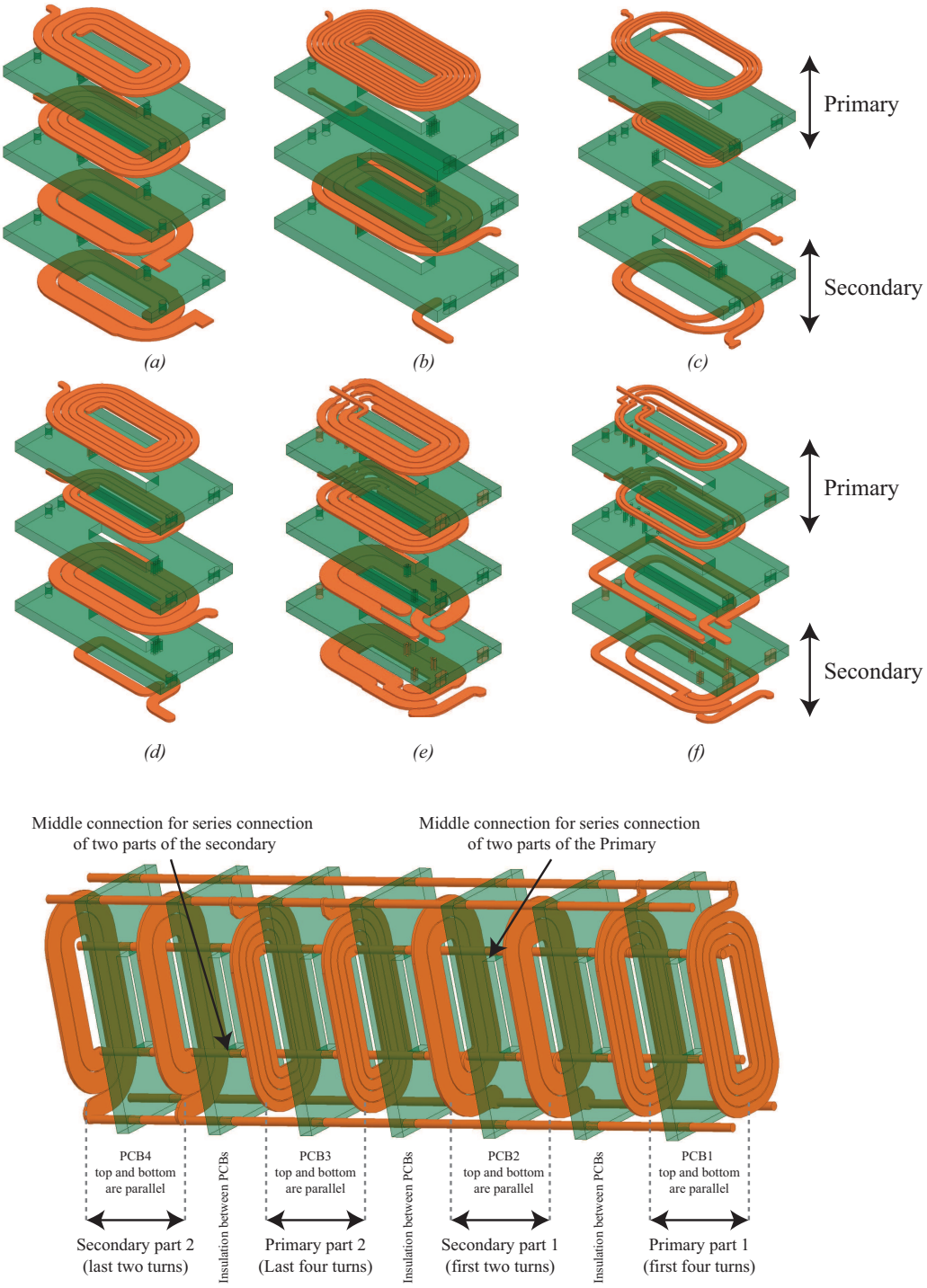
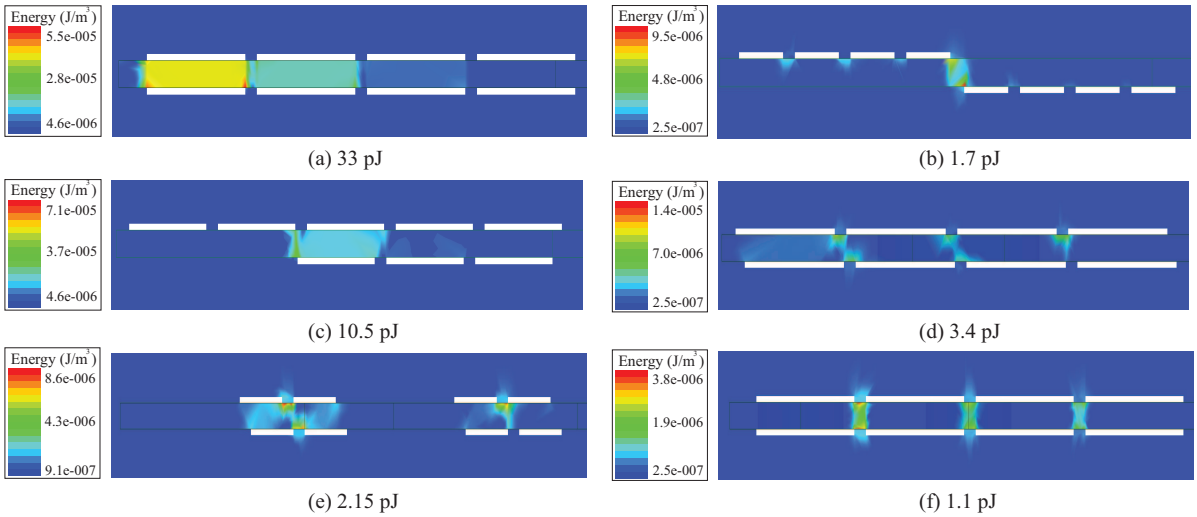


Fig. 10: The proposed improved winding layouts to reduce the parasitic capacitances in LLC converters: (a) Traditional spiral, (b) and (c) No overlapping, (d) Optimized overlapping, (e) Alternating, (f) Alternating & no overlapping and, (g) Zero voltage gradient winding layouts.



(a) 33 pJ (b) 1.7 pJ (c) 10.5 pJ (d) 3.4 pJ (e) 2.15 pJ (f) 1.1 pJ

Fig. 11: Intra-winding energy associated with one PCB of the proposed layouts. Each layout consist eight turns and 1V is distributed linearly between terminals of the layout: (a) Traditional spiral, (b) No overlapping, (c) Optimized overlapping, (d) Alternating, (e) Alternating & no overlapping, and (f) Zero voltage gradient winding layouts. It is clear that the proposed layouts have significantly less parasitic capacitance.

A. *No overlapping winding layouts*

Minimizing the overlapping area is the first approach to reducing the intra-winding capacitance. Fig 10 (b) and (c) show minimized overlapping winding layouts. These winding layouts are called *no overlapping* winding layouts through this paper. The energy stored in these winding layouts is proportional to the distributed capacitance between adjacent turns on the same side of PCB. The analytical expression for calculating the parasitic capacitance between adjacent turns is equal to the second term in (17). Fig. 11 (b) shows the intra-winding energy associated with one of these layouts. This figure shows that these layouts strongly reduce the intra-winding energy as the value of intra-winding energy is reduced from 33 pJ in the traditional design to 1.7 pJ. Regarding the inter-winding capacitance, these layouts offer double space between windings and reduce the value of static inter-winding capacitance. Although these layouts effectively mitigate the problem of intra-winding capacitances, they have higher DC resistance comparing to the traditional winding layout. In these layouts, only 50% of PCBs are used and consequently, the values of DC resistance is roughly twice of the traditional winding layout. Due to higher conduction loss, these designs are not suitable for high-efficiency LLC applications.

B. *Optimized overlapping winding layout*

The second winding layout which attempts to reduce the parasitic capacitance with less resistance increment is showed in the Fig 10 (d). The stored energy between overlapping traces depends on the voltage gradient of those traces. Therefore, the energy is not evenly distributed in the area between two layers, and more energy is stored between outer turns that have larger capacitance and voltage gradient. This feature is used in this layout to remove the overlapping area between the outer turns and effectively reduce the intra-winding capacitance. Removing the overlapping between these turns means that putting $(\frac{n}{2}+1)$ turns on one side and $(\frac{n}{2}-1)$ on the other side. For the PCBs with the odd number of turns, it means having $(\frac{n+1}{2})$ turns on one side and $(\frac{n-1}{2})$ turns on the other side. This winding layout is called *Optimized overlapping* winding layout in this paper. For even values of n the intra-winding energy and corresponding capacitance can be found by (19).

$$\begin{aligned} E_{intra} &= \int_0^{(\frac{\frac{n}{2}-1}{\frac{n}{2}+1})L} \frac{1}{2}\epsilon_0\epsilon_r \frac{W\times dx}{d} \times \Big(\frac{V_w(\frac{n-2}{n})}{(\frac{\frac{n}{2}-1}{\frac{n}{2}+1})L}x\Big)^2 \\ C_{intra} &= \Big[\frac{1}{3}\epsilon_0\epsilon_r\frac{W\times L}{d}\Big] \times \Big[(\frac{\frac{n}{2}-1}{\frac{n}{2}+1})(\frac{n-2}{n})^2\Big] \end{aligned} \tag{19}$$

Following the same procedure for odd values of n, the intra-winding capacitance associated with this condition is presented in the (20).

$$\begin{aligned} E_{intra} &= \int_0^{(\frac{n-1}{n+1})L} \frac{1}{2}\epsilon_0\epsilon_r \frac{W\times dx}{d} \times \Big[\frac{V_w(\frac{n-1}{n})}{(\frac{n-1}{n+1})L}x\Big]^2 dx \\ C_{intra} &= \Big[\frac{1}{3}\epsilon_0\epsilon_r\frac{W\times L}{d}\Big] \times \Big[(\frac{(n-1)^3}{n^2(n+1)})\Big] \end{aligned} \tag{20}$$

Assuming the total length of winding is equal to the traditional winding layout, DC resistance for each case is presented in the (21).

$$\begin{aligned} n = Even \qquad & R_{DC-Opt} = (\frac{n+2}{n})R_{DC-trad} \\ n = Odd \qquad & R_{DC-Opt} = (\frac{n(n+1)}{n^2+1})R_{DC-trad} \end{aligned} \tag{21}$$

In the above equations, $R_{DC-trad}$ is the DC resistance of traditional spiral design. Figures 12 and 13 show the normalized DC resistance and intra-winding capacitance of *Optimized overlapping winding layout* for different values of n. The base values for normalization are the DC resistance and intra-winding capacitance of traditional winding layout. These figures show that the value of intra-winding capacitance can be reduced effectively,

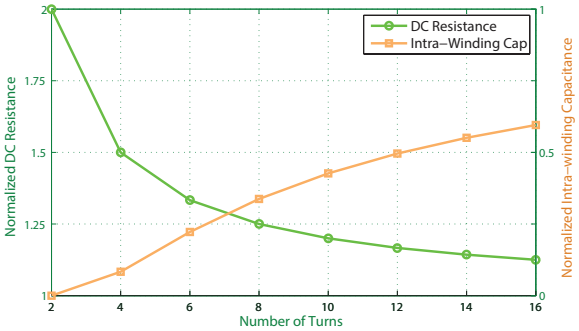


Fig. 12: Variations of DC resistance and intra-winding capacitance of *Optimized overlapping* winding layout for even values of n.

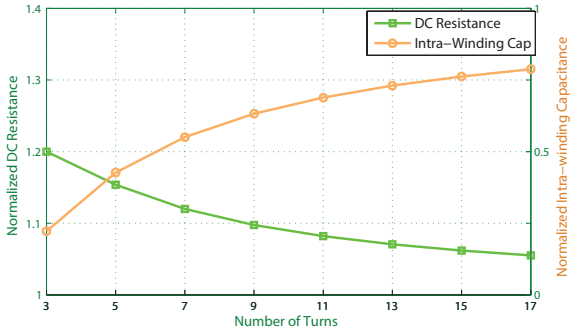


Fig. 13: Variations of DC resistance and intra-winding capacitance of *Optimized overlapping* winding layout for odd values of n.

without doubling the DC resistance. An eight turns winding layout with this strategy is showed in the Fig. 10 (d). The intra-winding energy distribution of this layout is showed in the Fig. 11 (c). This figure shows that in the case of eight turns PCBs, removing the overlapping area between first and last turns reduces the intra-winding capacitance by 69%. This result is in a very good agreement with (19). The percentage of increase in the DC resistance can be calculated using (21) which is equal to 25%. In comparison to the *no overlapping* winding layouts that have 100% more DC resistance, the DC resistance increment in this layout is just 25%. Although this layout proposes a significant capacitance reduction by small increment of resistance, the parasitic capacitance still is considerable and can lead to voltage regulation problems. Therefore, more optimized winding layouts should be investigated to strongly reduce the parasitic capacitance while not letting the resistance to increase.

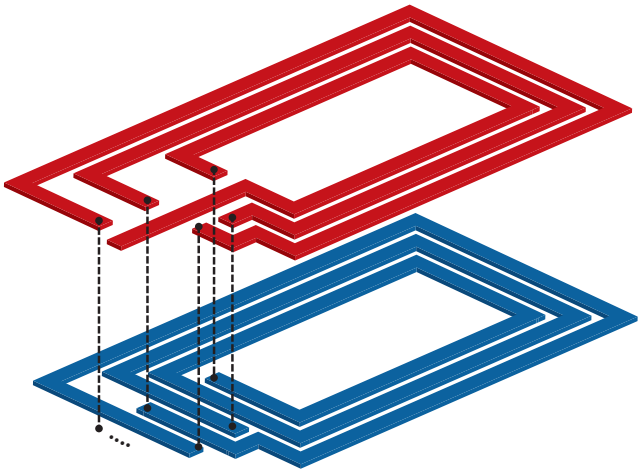
C. Alternating winding layout

No overlapping and *Optimized overlapping* winding layouts are based on the overlapping minimization principle. Although effective in mitigating the intra-winding capacitance, these winding layouts sacrifice DC resistance to mitigate the intra-winding capacitances. The intra-winding capacitance also can be minimized by reducing the voltage gradient between overlapping traces. Minimizing voltage gradients between large overlapping traces reduces the intra-winding energy and consequently the intra-winding capacitor.

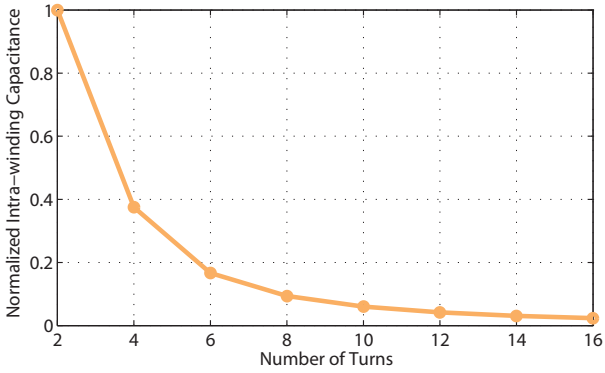
One way to reduce the voltage gradient between overlapping traces is illustrated in the Fig. 14 (a). This winding layout is called *Alternating* winding layout in this paper. In this layout, the overlapping traces are two successive turns. In other words, after each turn, the next turn is on the other side. These turns are connected through VIA. For this layout, the intra-winding energy can be calculated by (22).

$$E_{intra} = \int_0^L \frac{1}{2}\epsilon_0\epsilon_r \frac{W \times dx}{d} \times (\frac{V_w}{\frac{n}{2}})^2 = \left[\frac{1}{2}\epsilon_0\epsilon_r \frac{W \times L}{d} V_w^2 \times (\frac{4}{n^2})\right]$$
$$C_{intra} = \left[\frac{1}{3}\epsilon_0\epsilon_r \frac{W \times L}{d}\right] \times \left[\frac{6}{n^2}\right] \quad (22)$$

The above equation shows that this winding layout reduces the value of intra-winding capacitance by the factor of $\frac{6}{n^2}$. Fig. 14 (b) presents the intra-winding capacitance of this layout for different



(a)



(b)

Fig. 14: (a) *Alternating* winding layout with terminals at the outer edges of PCB and (b) Variations of intra-winding capacitance of *Alternating* winding layout for even values of n.

values of n and shows that the value of intra-winding capacitance rapidly decreases by increasing the number of turns. Regarding the DC resistance, this winding layout has no increment as all of the available PCB is used for copper traces. Fig. 10 (e) shows an eight turns *Alternating* winding layout. For the ease of connecting to other PCBs, the winding is started from the middle, and the terminals are at the edges of the PCB. The intra-winding energy distribution of this layout also is showed in the Fig. 11 (d). This figure shows that an eight turns *Alternating* winding layout has 10 times less intra-winding energy than the traditional winding layout which is in a good agreement with (22). In comparison to the previous designs, this layout reduces the intra-winding capacitance without sacrificing the DC resistance. Although this layout is a suitable candidate for wide-range and efficient LLC converters, it does not have any superiority in terms of the inter-winding capactitance. Thereofore, other winding layouts should be investigated to find an optimum layout that minimize both types of the parasitic capacitances.

D. Alternating & No overlapping winding layout

Minimized overlapping strategy also can be used to reduce the value of inter-winding capacitance. On this basis, a winding layout, *Alternating & no overlapping* winding layout, with minimized overlapping of primary and secondary is showed in the Fig. 10 (f). This layout uses the alternating layout to reduce the intra-winding capacitance and avoids any overlapping between primary and secondary to minimize the inter-winding capacitance. Therefore, this transformer minimizes both intra and inter-winding capacitances. Due to the alternating layout and lower overlapping area between the traces of the same winding, the intra-winding capacitance of this layout is very low. Fig. 11 (e) shows the intra-winding energy of this layout which is roughly 15 times less than traditional layout. Since the overlapping of primary and secondary is avoided in this structure, this layout also has lower inter-winding capacitance. On the downside, this layout only uses 50% of PCB and therefore has twice DC resistance. More importantly, this layout has very high AC resistance due to the proximity effect. Therefore, it makes a lot of conduction loss and is not suitable for high efficiency LLC converters. This layout will be discussed more in the next section.

E. Zero Voltage gradient winding layout

The final proposed winding layout for solving the parasitic capacitance problem is called *Zero voltage gradient* layout. In order to explain this winding method, a $8:4$ transformer that is realized using the double layers PCBs is showed in Fig. 10. (g). There are four different PCBs (two double sided PCBs for primary and two double sided PCBs for the secondary). This figure shows that the eight turns of the primary are splitted into two parts. The first four turns of the primary are duplicated on both sides of the first PCB of primary. The top and bottom layers of this PCB are connected in parallel which means that this PCB has four turns out of eight turns of the primary. Since the top and bottom turns of this PCB are identical and connected in parallel, they have the same voltage and there is no voltage gradient between the overlapping turns. This condition also can be seen from the direction of the turns in this PCB. The four remaining turns of the primary are duplicated on both sides of second PCB of the primary. Like the first PCB, the top and bottom layers of this PCB also are connected in parallel. The first four turns that are on the first PCB then are connected in series to the four turns of second PCB via a middle connection, making an eight turns primary winding. The same is true for the secondary winding. Therefore, the key idea here is that the top and bottom layers of each PCB should be identical and connected in parallel to achieve zero voltage gradient and minimize the parasitic capacitance. The proposed idea is implemented in the Fig. 10 (7) (g) by dividing each winding into two portions and duplicating each portion on top and bottom side of a separate PCB. Then connecting two PCBs with a middle connection. In the general case, the proposed idea can be extended to dividing winding into any even number of groups. The following shows the steps that are required to implement this idea:

1) Each winding should be splitted into two (or any even number of) groups and each group should be duplicated on both sides of a separate PCB. The minimum number of required PCBs for each PCB is equal to the number of groups.
2) The top and bottom layers of each PCB should be connected in parallel.
3) Different PCBs should be placed separately to avoid the voltage gradient between them. All different PCBs should be

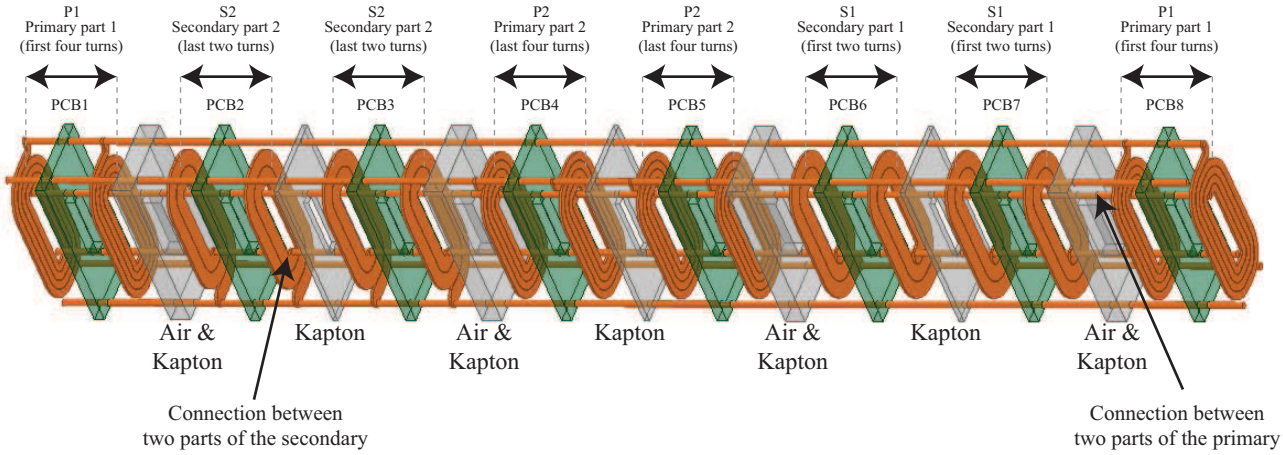


Fig. 15: *Zero voltage gradient* transformer with the $P1S1S1P2P2S2S2P1$ structure. It is clear that all overlapping traces of the same winding have zero voltage gradient.

connected in series to make a complete winding. For some of PCBs, Middle connection should be used to connect two successive PCB. The number of required middle connections is equal to half of the number of PCBs.

It can be seen that the above rules are applied to the transformer of Fig. 10 (g). For this case, each winding is divided into two groups and two PCBs are required for each winding to complete the winding (one PCB for each group). The intra-winding energy distribution of a PCB with this layout is showed in the Fig. 11 (f). In comparison to the traditional winding, the value of intra-winding energy is reduced from 33 pJ to just 1.1 pJ, with the same overlapping area and without any compromise on the DC resistance. This reduction in the parasitic capacitance is even more than the minimized overlapping winding layouts that have double conduction loss.

As mentioned before, the minimum number of PCBs that are required for each winding in this method is equal to the number of portions that the winding is divided. If the core windows can accommodate more layers, it is desirable to add extra layers in parallel to reduce the resistance. For example in Fig. 15, the windings of the same transformer are realized by using four PCBs (two PCB in parallel for each portion of windings). The PCBs that are connected in parallel are identical and both have the same portion of winding. Therefore, they also have the same voltage distribution. This characteristic can be used to reduce the inter-winding capacitance. Due to zero voltage gradient between these PCBs, they can be placed very close to each other without being worry about increasing the intra-winding capacitance or violating the electrical clearance which saves space in the limited height of the core windows. This space can be used to increase the number of layers or to increase the separation distance in the primary and secondary intersections to reduce the inter-winding capacitance. This advantage is showed in the Fig 15. This figure clearly shows that similar PCBs are separated just by one Kapton layer, providing more separation distance for intersections of primary and secondary. Therefore, this winding layout not only gives the minimum intrawindng capacitance, but also provides the opportunity to reduce the interwinding capacitance. The benefits of this winding layout can be summarized as the following:

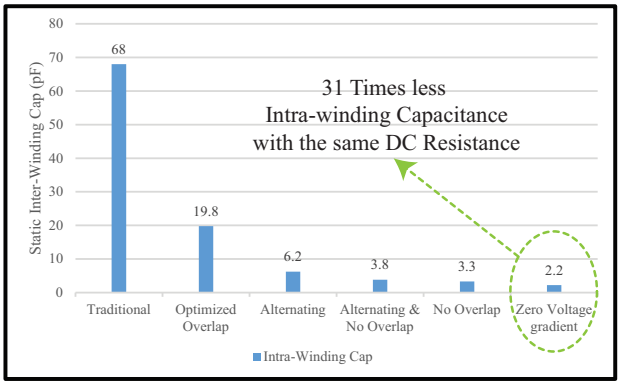
1) Having extremely low intra-winding capacitance due to zero voltage gradient between overlapping traces.
2) No increment in the value of DC resistance. The same DC resistance of traditional winding layout.
3) Identical PCBs can be placed with very low separation distance without increasing the intra-winding capacitance. Therefore, there is more space to be used in the intersections of primary and secondary, resulting in a less inter-winding capacitance.

Due to very low parasitic capacitance, this layout can resolve both CM noise and light-load voltage regulation problem in the LLC converter, while at the same time gives low resistance which ensures the high full-load efficiency. Therefore, this layout is very suitable to be employed in the LLC resonant converters.

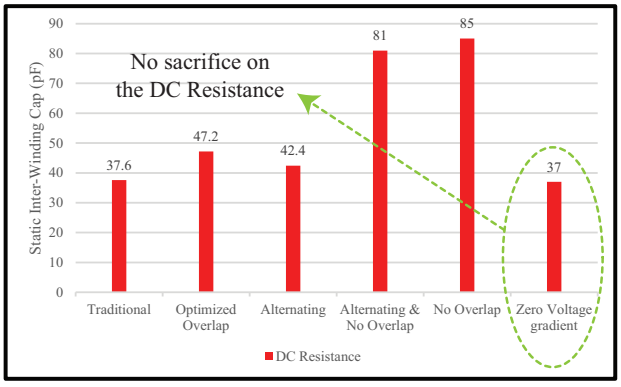
F. Comparison of the proposed winding layouts

In the previous parts, six improved winding layouts are proposed to minimize the parasitic capacitance of PT and consequently, solve the problems due to the parasitic capacitance in the LLC resonant converter. Among the proposed winding layouts, layouts that reduce the parasitic capacitance by decreasing the overlapping have higher DC resistance. On the other hand, the designs that minimize the parasitic capacitance by reducing the voltage gradient have the benefit of using all the available space and therefore do not compromise DC resistance. The DC resistance and intra-winding capacitance of different winding layouts are compared in the Fig. 16 (a) and (b). Fig. 16 (a) shows that all of the proposed winding layouts have considerably lower intra-winding capacitance than traditional spiral layout.

No overlapping layouts can strongly mitigate the parasitic capacitance and solve the regulation problem. However, they also double the DC resistance which leads to higher conduction loss. *Optimized overlapping* layout is the optimized version of *No overlapping* layouts that reduces a big portion of parasitic capacitance by a small increase in the resistance. However, it is not as effective of *No overlapping* layout and since wide output regulation requires very low parasitic capacitance, it may not solve the regulation problem. *Alternating* layout also strongly reduces the intra-winding capacitance without increasing the DC resistance. Therefore, this layout can be used to resolve the regulation problem without compromising the efficiency. However, in terms of CM noise it does not have any advantage over the traditional layout. In order to reduce both intra- and inter-winding capacitances, *Alternating & no overlapping* layout is proposed. Although this layout effectively reduce the parasitic capacitances, it has significantly higher AC resistance in comparison to other layouts which will be discussed more in the next section. Among different layouts,



(a)



(b)

Fig. 16: Parasitic elements comparison of different winding layouts: (a) Intra-winding capacitance and (b) DC resistance

Zero voltage gradient layout offers the minimum intra-winding capacitance without any increment in the DC resistance. Reducing the intra-winding capacitance significantly enhance the converter performance and mitigate the regulation problem. In terms of inter-winding capacitance, this layout also provides the lowest inter-winding capacitance. Minimising the inter-winding capacitance not only reduces the CM noise, but also enhance the regulation. Therefore, this layout is the best among the proposed layouts.

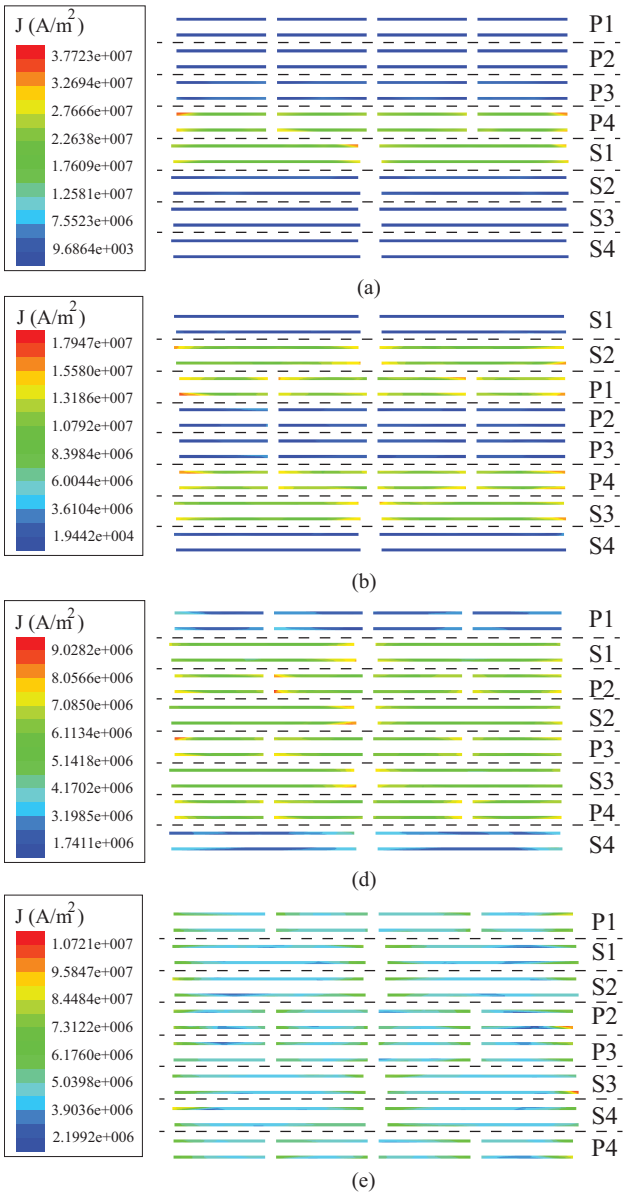


Fig. 17: Current density in different arrangements: (a) PPPPSSSS (NI), (b) SSPPPPSS, (c) PSPSPSPS (FI), and (d) PSSPPSSP. It is evident that PSSPPSSP structure leads to an even distribution of the current between layers and provides the best AC resistance.

IV. Arrangement Tradeoff Analysis

In the previous section, improved winding layouts are proposed to significantly reduce the parasitic capacitance and attenuate the CM noise and solve the voltage regulation problem in the LLC resonant converter. In addition to the winding layout, the structure of the transformer strongly affect the parasitic elements. It is interesting to note that there is a trade-off between intra-winding capacitance, AC resistance and leakage inductance against the inter-winding capacitance. The values of intra-winding capacitances, AC resistances, and leakage inductances decrease by using interleaved structures. On the other hand, the inter-winding capacitance is proportional to the number of intersections between primary and secondary which increases in the interleaved structure. Most of the proposed winding layouts in the previous section can effectively solve the intra-winding problem. Besides, the leakage inductances are inherently small in PTs comparing to the wire wound transformers and also the primary leakage inductance is capable of being absorbed by the series inductor. For these reasons, the trade-off analysis in finding the optimum arrangement is only made based on AC resistance and inter-winding capacitance. On this basis, the optimum structure is the one that minimizes the AC resistance with the minimum number of intersections between primary and secondary.

Fig. 17 shows the current density in the transformer with four layers of primary and secondary in different structures. This figure shows that the best current distribution between layers happens in the $PSSPPSSP$ structure. In comparison to the fully interleaved structure, the number of intersections has reduced from seven to four, meaning the value of inter-winding capacitance is reduced roughly by 43%. This reduction in the parasitic capacitance can significantly attenuate the CM noise in LLC converters. The comparison of different structures regarding parasitic elements are presented in the figures 18 and 20.

It should be noted that both $SPPSSPPS$ and $PSSPPSSP$ have similar results in terms of AC resistance and inter-winding capacitance. Sine the number of primary and secondary intersections are equal, they have similar inter-winding parasitic capacitance. The similarity in the result of AC resistance also can be explained by finding the MMF distribution along the wingdings as both of those arrangements have the same MMF distribution. The MMF distribution of these arrangements are showed in Fig. 19 (a). If the core window can accommodate more layers, other portions of

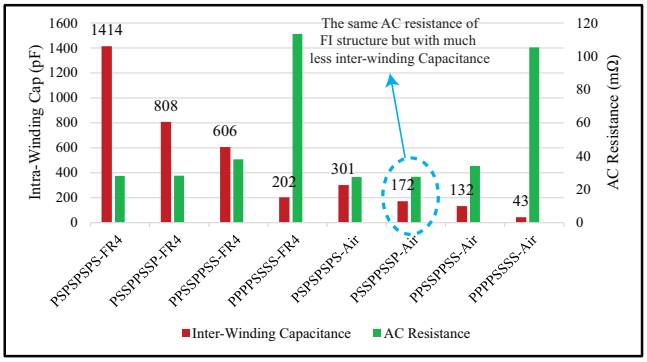


Fig. 18: The comparison of AC resistance and inter-winding capacitance of an eight layers transformer with traditional spiral windings in different structures.

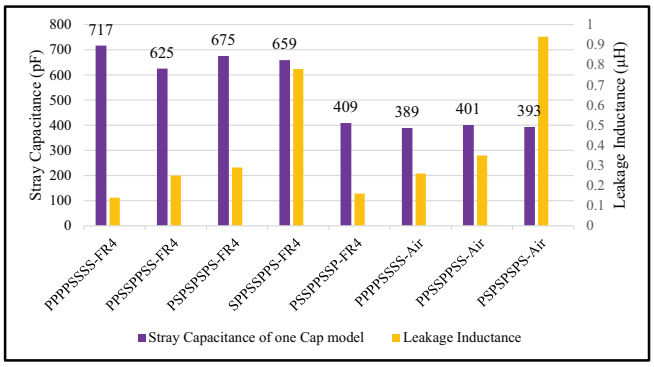


Fig. 20: The comparison of leakage inductance and primary parallel stray capacitance of an eight layers transformer with traditional spiral windings in different structures.

interleaving also is viable with the proposed winding layouts and arrangements. For example, Fig. 19 (b) shows the same transformer with the $PSSPPSSPPSSPPSSP$ arrangement.

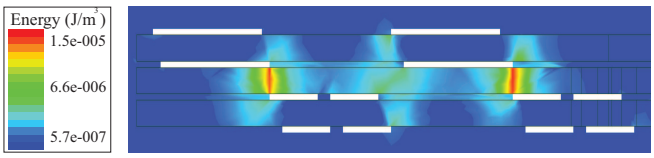


Fig. 21: Inter-winding energy of one intersection between windings in Alternating & No overlapping layouts.

The proposed winding layouts also are investigated with different structures and in all cases the proposed arrangement gives the best results. The only exception is the *Alternating & No overlapping* winding layout which has significantly larger AC resistance in all arrangements. Table III shows the ratio of AC to DC resistance of this layout in different structures. This table shows

TABLE III: The ratio of AC resistance to DC resistance of *Alternating & No overlapping* winding layout in different structures

Arrangement	R_{ac}/R_{dc}
$PPPPSSSS$	168.6/48.1
$PPSSPPSS$	184.3/48.1
$PSPSPSPS$	212.0/48.1
$PSSPPSSP$	201.5/48.1

that the interleaving does not solve the proximity effect. Since the primary and secondary turns do not meet each other, primary and secondary MMF do not cancel each other and the proximity effect leads to high ratio of AC to DC resistance. Fig. 21 shows the inter-winding energy of *Alternating & No overlapping* winding layout. This figure clearly shows that even with no overlapping between primary and secondary, still there are some capacitive coupling between windings due to the fringing of electric field. Indeed, even with no overlapping between primary and secondary, the value of inter-winding capacitance is half of the traditional winding layout. Considering the problem of AC resistance and the fact that inter-winding capacitance still has large value, the minimization of overlapping between primary and secondary is not a practical way to mitigate the inter-winding capacitance problem. Instead, the inter-winding capacitance should be minimized through optimizing the structure, increasing the separation distance between windings and, using the low permeability materials in the intersections.

Having the improved winding layouts and the optimized structure with low AC resistance and inter-winding capacitance, now we are able to fabricate very low parasitic capacitance PTs for

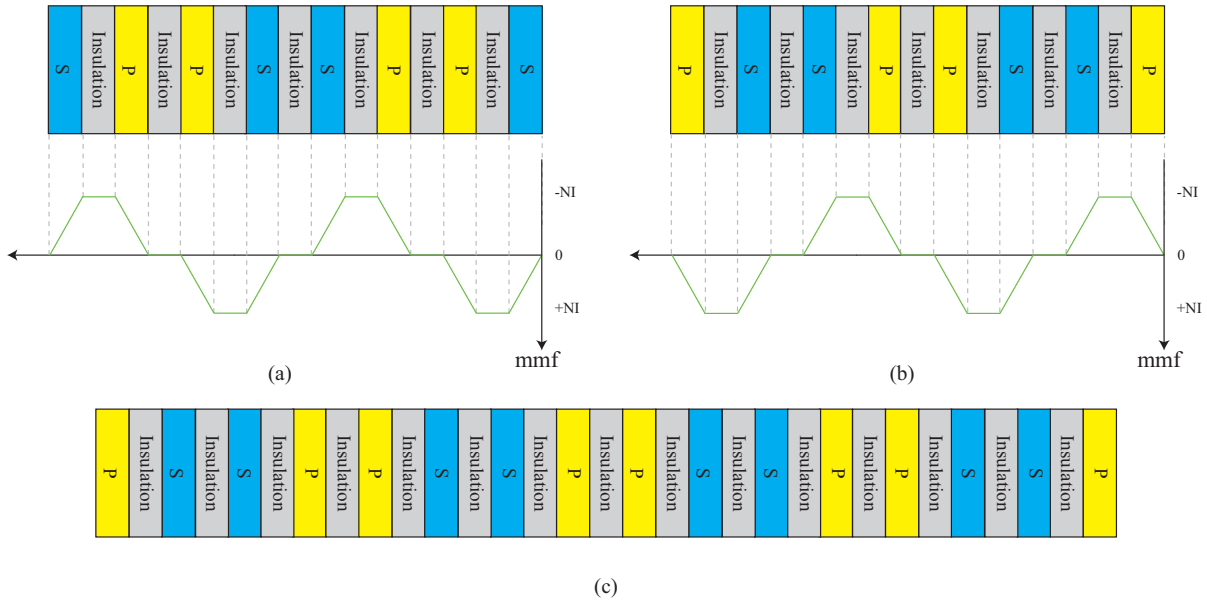


Fig. 19: (a) Comparison of the MMF distribution along the winding in $PSSPPSSP$ and $SPPSSPPS$ arrangements and (b) Similar interleaving method with the double number ofr PCBs.

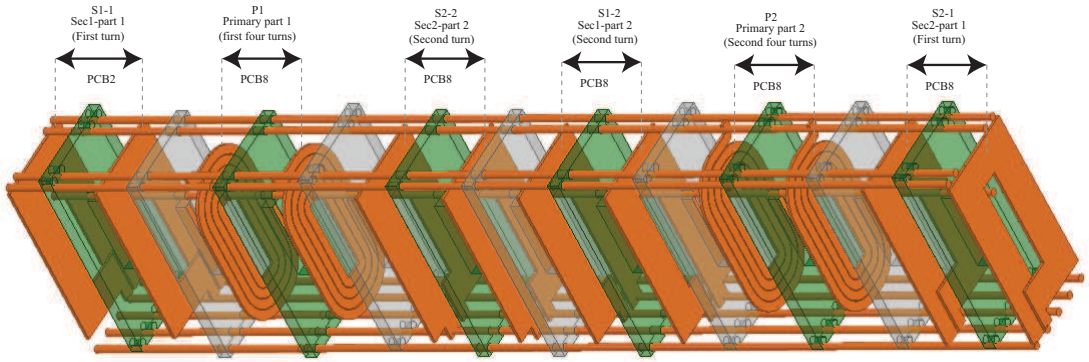


Fig. 22: A 8:2:2 centre-tapped planar transformer with *zero voltage gradient* winding layout and b) the connection of PCBs.

high efficiency LLC resonant converter with wide output voltage. These transformers can be used to resolve both CM noise and voltage regulation problem in the LLC resonant converter.

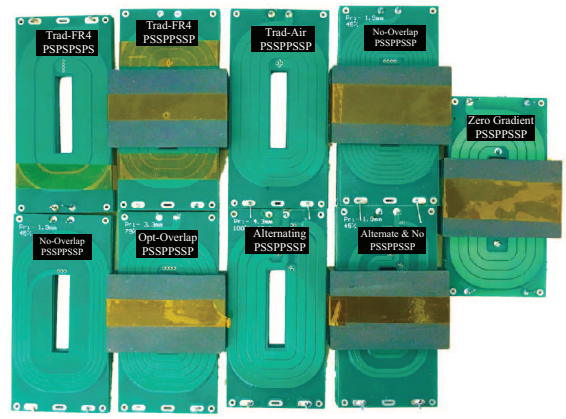
A. Application of the Proposed Winding Layouts in the Centre-Tapped PTs

All of the proposed winding layouts also can be implemented in the centre-tapped planar transformers. The proposed air separation method can be employed between PCBs of different windings to reduce the inter-winding capacitance. On the other hand, the PCB layouts that are presented in the paper can be used to minimize the intra-winding capacitance between top and bottom layers of each PCB. winding arrangement of the center-tapped PTs should be selected by considering the passive losses in the non-conducting secondary. Finding the optimized arrangement of the center-tapped PTs falls out of scope of this paper and will be addressed in the future work. However, In order to show the applicability of the proposed methods on centre-tapped planar transformers, Fig. 22 (a) shows a 8:2:2 centre-tapped planar transformer that is realized using the air separation method and *zero voltage gradient* layout. As it is clear from this figure, there is no voltage gradient between top and bottom layers of each PCB which minimizes the intrawinding capacitance of the windings. The inter-winding capacitance between different layers also is attenuated using the air separation method.

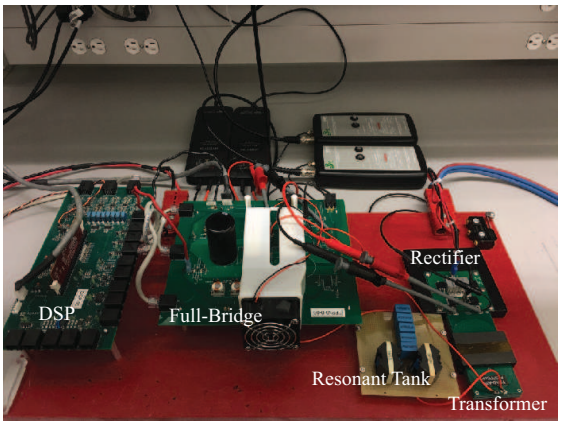
V. Experimental Results

To verify the theoretical hypothesis, the winding layouts under investigation were manufactured (total of 6) and employed in a 1.2kW LLC resonant converter. The experimental results show that the proposed PTs have extremely lower parasitic elements in comparison to the conventional PTs which mitigates the light-loading voltage regulation problem and also ensures high full-load efficiency by minimizing AC resistance and inter-winding capacitance. The specification of the converter and PTs are provided in table IV.

Fig. 23 (a) and (b) show the prototypes of the special PTs under study and the LLC resonant converter platform, respectively. Fig. 24 (a) shows the frequency response of different transformers with the secondary open. As long as the leakage inductances are negligible in comparison to the magnetizing inductance, the equivalent capacitor in this condition is equal to C_{stray}. Considering the fact the open circuit inductance is the same in all conditions, Fig. 24 confirms that the proposed transformers have significantly lower stray capacitance. Fig. 24 (b) shows the stray capacitance of different layouts. Among different layouts, *zero voltage gradient* winding layout has the lowest primary parallel stray capacitance. In comparison to the traditional FI transformer, this transformer



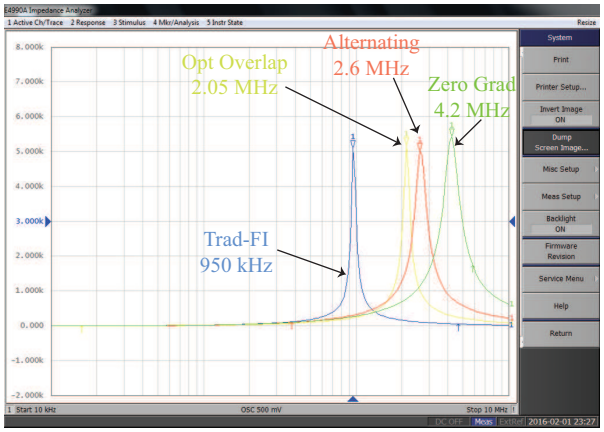
(a)



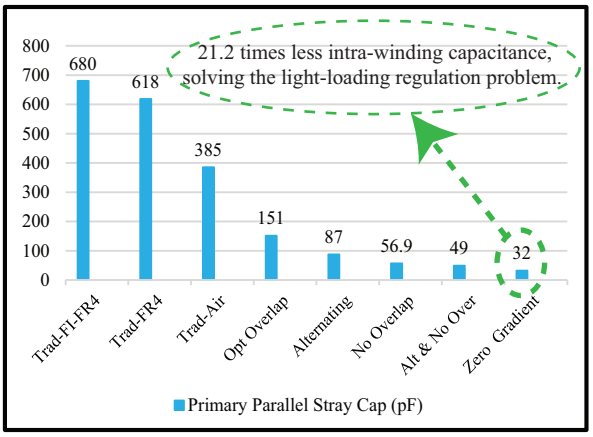
(b)

Fig. 23: Experimental prototypes: (a) Transformers prototypes and (b) LLC resonant converter platform

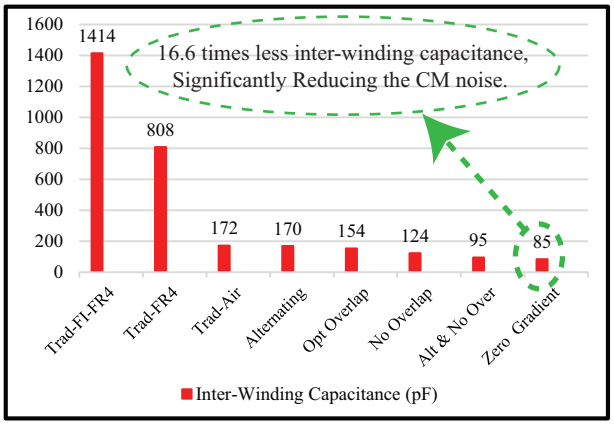
has 21.2 times less stray capacitance. Fig. 24 (c) shows the inter-winding capacitance of the proposed transformers. This figure shows that using an optimized structure and replacing $FR4$ with



(a)



(b)



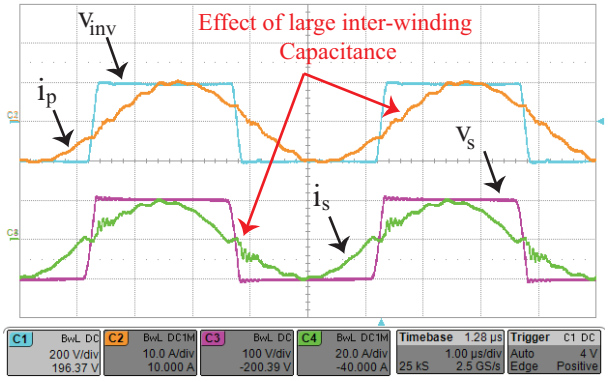
(c)

Fig. 24: Parasitic values of the prototypes: (a) frequency response, (b) inter-winding capacitance, and (c) equivalent primary stray capacitance.

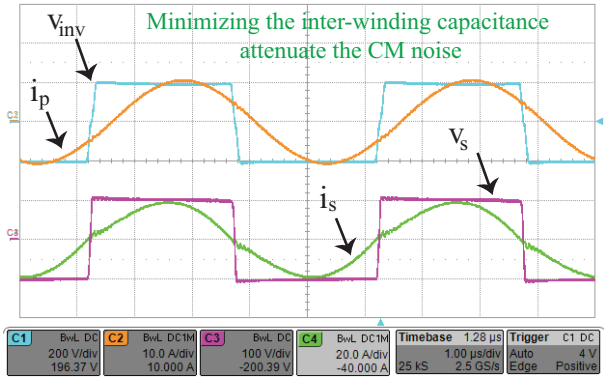
TABLE IV: Parameters definition

Converter Prameters		Transformer Prameters	
Parameters	Value	Parameters	Value
V_{in}	200 V	N_p/N_s	2:1 (8:4)
V_{out}	96 V	Core	ELP 58/11/38
P_{out}	1200 W	PCB Thickness	0.6mm
f	200 kHz	Copper Thickness	4 Oz

air significantly reduces the inter-winding capacitance. Among different layouts, *zero voltage gradient* winding layout again has the best result as its inter-winding capacitance is 16.6 times less than traditional FI structure. Fig. 25 (a) and (b) show the full-load waveforms of LLC resonant converter with the traditional PT and the proposed *zero voltage gradient* transformer. Here, the inverter voltage is the output voltage of the full-bridge inverter. Comparing the waveforms, it is clear that reducing the inter-winding capacitance reduces the high-frequency currents and considerably

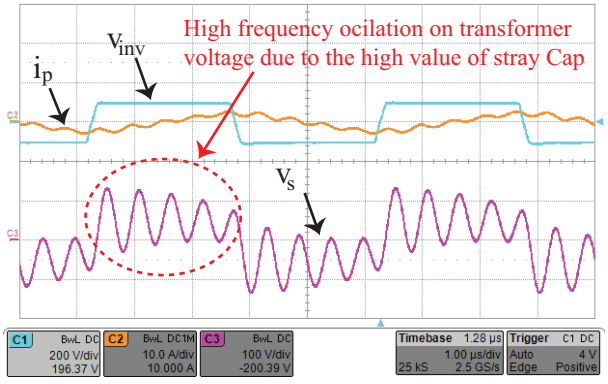


(a)

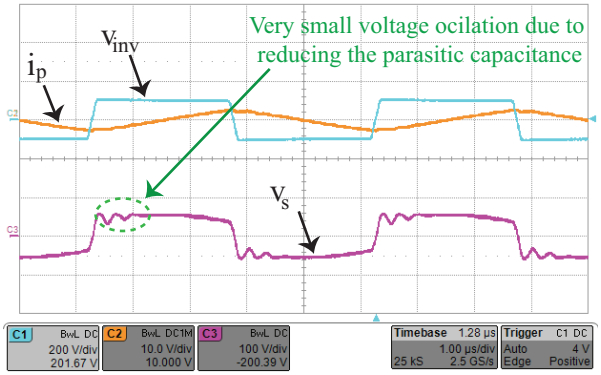


(b)

Fig. 25: Waveforms in the LLC resonant converter under full-loading condition for different transformers: inverter voltage (Ch1), primary current (Ch2), transformer secondary voltage (Ch3), and transformer secondary current (ch4). (a) Traditional-FI and (b) *zero voltage gradient* transformers. It is clear that reducing the inter-winding capacitances has attenuated the CM noise problem significantly.

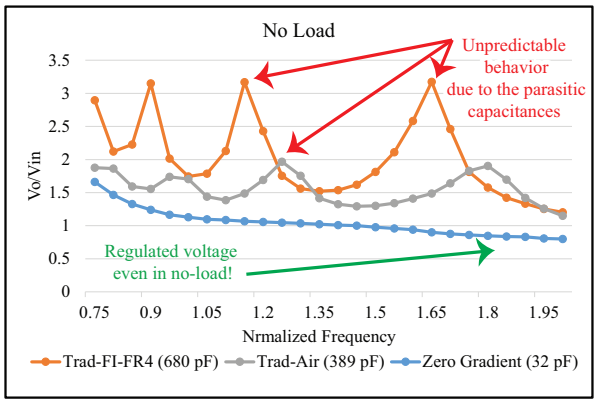


(a)

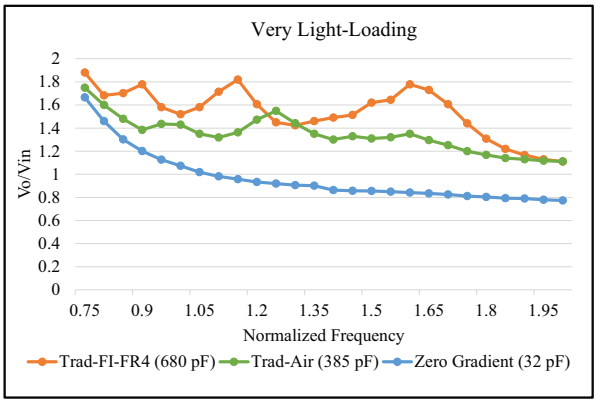


(b)

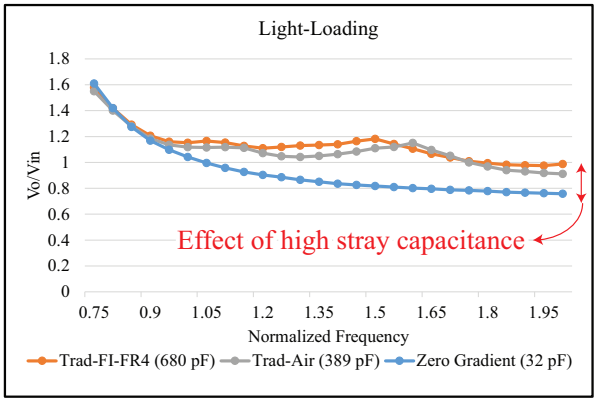
Fig. 26: Waveforms in the *LLC* resonant converter under no-loading condition for different transformers: inverter voltage (Ch1), primary current (Ch2), and transformer secondary voltage (Ch3). (a) Traditional-FI and (b) *zero voltage gradient* transformers. Reducing the stray capacitances has improved the no-load voltage waveform and successfully mitigated the light-load voltage regulation problem.



(a)



(b)



(c)

Fig. 27: Converter voltage gain characteristic with different transformers at a) no load, b) very light load and, c) light load. The conventional PT has serious regulation issues for all cases and the proposed *Zero voltage gradient* layout solves this problem by achieving an extremely low capacitance.

improves the current waveforms. Fig. 26 (a) shows the transformer voltage in the no-load condition with the traditional PT. This figure shows that high stray capacitance distorts the transformer no-load voltage and it cannot be considered as square-shaped. This distorted waveform makes serious problems in controlling output voltage in the no-load and light-load condition which cannot be predicted with FHA. On the other hand, Fig. 26 (b) shows the no-load voltage of converter with the proposed *zero voltage gradient* transformer. This figure shows that even under no-load condition, the transformer voltage still is square shaped.

Since large parasitic capacitances distort the transformer no-load voltage, FHA fails to consider all issues introduced bythese parasitic capacitances and accurately predict the output voltage behavior. Fig. 27 (a), (b), and (c) compare the voltage characteristics of the converter with different transformers in three light-load conditions. It is clear that large stray capacitance leads to an unpredictable voltage behavior under the no-load condition. Fig. 27 (b) and (c) show increasing the load can somehow improve the situation. However, the voltage behavior still is unpredictable. In addition to the unpredictable behavior, the converter cannot regulate for low output voltages as is showed in the Fig. 27 (c). Minimizing the parasitic capacitance can avoid these problems and enables the converter to regulate output voltage. It is clear that for the

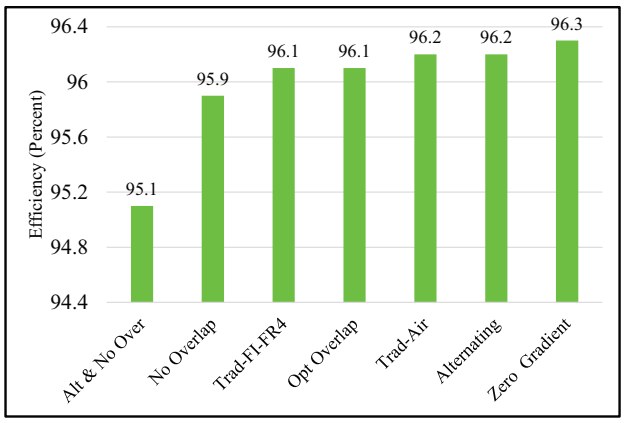


Fig. 28: Full-load efficiency of the converter at resonant frequency with different transformers.

same sweeping frequency, the converter with *zero voltage gradient* transformer can provide wider ranges of output and regulate the output voltage.

PTs also are compared regarding the converter efficiency. Fig. 28 shows the full-load efficiency of the converter at resonant frequency with different transformers. This figure shows that *zero voltage gradient* transformer has the highest efficiency between different transformers. It is mainly due to low resistance and low CM noise. The efficiency for other transformers that have higher resistance is slightly lower. In the case of *Alternating* & *No overlapping* winding layout, as it is stated in the previous sections, the interleaving does not improve the AC resistance, and this transformer has much higher AC resistance. Therefore, the efficiency of this transformer is considerably lower than other transformers. As a result, the non-overlapping strategy is not a suitable layout for high-efficiency applications.

VI. Conclusion

This paper presented the problems associated with the parasitic capacitance of PTs in LLC resonant converters and proposed a mitigation strategy to reduce the parasitic capacitance and improve the converter performance. It was shown that the high inter-winding capacitance makes the CM noise problems while the parallel stray capacitance leads to voltage regulation problems in the light-load condition. In order to overcome these problems, a systematic analysis was performed, and six PT winding layouts were introduced and benchmarked with a traditional design. The proposed winding layouts were compared regarding parasitic capacitances and resistance with the aid of analytical equations. As a result of the investigation, an optimized structure with minimum AC resistance and inter-winding capacitance was found and verified by FEA and experimental results. The proposed winding layouts and structure were used to manufacture PTs with very low parasitic capacitance. While all of the proposed transformers significantly reduce the parasitic capacitances, the proposed *Zero voltage gradient* layout has the best results as it has 21.2 times less primary stray capacitance and 16.6 times less inter-winding capacitance. This structure reduces the stray and inter-winding capacitances from $618pF$ and $1414pF$ to $32pF$ and $85pF$, respectively. Another advantage of this transformer is that it reduces the parasitic capacitance without increasing the resistance and has the lowest parasitic capacitances and resistance at the same time.. This significant parasitic capacitance reduction has a tangible effect on the performance of LLC resonant converter. The experimental results of employing the proposed transformers in a 1.2 kW LLC resonant converter shows that not only the proposed transformers have enhanced the performance and efficiency of the converter by minimizing AC resistance and inter-winding capacitance, but also have mitigated the voltage regulation problem and enabled the converter to regulate the output voltage even in the no-load condition.

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